

Steve (Sung-Mo) Kang
Dean, Baskin School of Engineering
Professor, Department of Electrical Engineering
University of California, Santa Cruz

June 20, 2005

EMPLOYMENT HISTORY

- 2001- Dean, Baskin School of Engineering, UC Santa Cruz, Santa Cruz
- 2004- Professor Above-Scale, Electrical Engineering, UC Santa Cruz
- 2001-2004 Professor Highest Step, Electrical Engineering, UC Santa Cruz
- 2003-2005 Chaired Visiting Professor, Korean Advanced Institute of Science and Technology (KAIST)
- 2001- Professor Emeritus, Electrical and Computer Engineering, Univ. of Illinois at Urbana-Champaign
- 1989-2000 Professor, Electrical and Computer Engineering, Univ. of Illinois at Urbana-Champaign
- 1989-2000 Research Professor, Coordinated Science Laboratory, Univ. of Illinois at Urbana-Champaign
- 1990-2000 Professor, Computer Science, Univ. of Illinois at Urbana-Champaign
- 1990-2000 Research Professor, Beckman Institute, Univ. of Illinois at Urbana-Champaign
- 1993-1996 Founding Director, Center for ASIC Research and Development, University of Illinois at Urbana-Champaign
- 1995-2000 Head, Department of ECE, Univ. of Illinois at Urbana-Champaign
- 1985-1989 Associate Professor, Electrical and Computer Engineering, Univ. of Illinois at Urbana-Champaign
- 1985-1989 Research Associate Professor, Coordinated Science Laboratory
- 1989 Visiting Professor, Swiss Federal Institute of Technology at Lausanne
- 1998 Humboldt Visiting Professor, Technical University of Munchen, Germany, Summer 1998
- 1997 Humboldt Visiting Professor, University of Karlsruhe, Germany, Summer 1997
- 1982-1985 Supervisor, AT&T Bell Laboratories, Murray Hill, NJ
- 1977-1982 Member of Technical Staff, AT&T Bell Laboratories, Murray Hill, NJ
- 1977-1984 Visiting Faculty Member, Rutgers University, Piscataway, NJ
- 1975-1977 Assistant Professor, Rutgers University, Piscataway, NJ

EDUCATION

1975	Ph.D. Electrical Engineering	Univ. of California at Berkeley
1972	M.S. Electrical Engineering	State Univ. of New York at Buffalo
1970	B.S. Electrical Engineering	Fairleigh Dickinson Univ., Teaneck, NJ (Summa Cum Laude)

HONORS AND AWARDS

Myril B. Reed Best Paper Award, 1979

AT&T Bell Laboratories Exceptional Contribution Award, 1984

Best Paper Award, International Conference on Computer Design, 1987

Listed in Incomplete List of Teachers Ranked as Excellent by Students, Univ. of Illinois, 1987, 1993

IEEE Fellow, 1990

AAAS Fellow, 1997

ACM Fellow, 2000

IEEE Computer Society Meritorious Service Award, 1990

IEEE Computer Society Distinguished Service Award, 1990

Associate in the Center for Advanced Study, UIUC, 1991-1992

Founding Editor-in-Chief, IEEE Transactions on VLSI Systems, February 1992 - December 1994

IEEE Darlington Best Journal Paper Award, May 1993

Republic of China National Science Council Distinguished Lecturer, June 1993

SRC Inventor Recognition Award 1993, 1996, 2002

IEEE Circuits and Systems Society Meritorious Service Award, 1994

IEEE Circuits and Systems Society Distinguished Lecturer, 1994-1997

IEEE LEOS Conference Best Student Paper Award (Senior Author), 1995

University of Illinois Charles Marshall Senior University Scholar, 1995

IEEE Graduate Teaching Technical Field Award (worldwide award), 1996

Alexander von Humboldt Research Award for Senior U.S. Scientists, 1996

Co-Editor, Series in Advances in Design and Analysis of VLSI Systems, Elsevier Science Publishers B. V.

Foreign Member, National Academy of Engineering of Korea, 1997

IEEE Circuits and Systems Society Technical Achievement Award, 1997

Korea Broadcasting System (KBS) Compatriot Award, 1998

IEEE Circuits and Systems Society Golden Jubilee Medal, 1999

SRC Technical Excellence Award, 1999

22nd EOS/ESD Symposium Best Student Paper Award (Senior Author), 2000

IEEE Millennium Medal, 2000

Distinguished Alumnus Award in Electrical Engineering, UC Berkeley, 2001

Low Power Design Contest Award, International Symposium on Low Power Electronics and Design, 2001

IEEE Solid-State Circuits Society Distinguished Lecturer, 2002-

IEEE Circuits and Systems Society Distinguished Lecturer, 2003-

Chancellor's Stellar Service Award, UC Santa Cruz, 2003

IEEE Circuits and Systems Society Mac Van Valkenburg Award, 2005

Listed in Who's Who in America, Who's Who in Technology, Who's Who in Engineering, Who's Who in Midwest, American Men and Women of Science

RECENT (2002-PRESENT) GOVERNMENT AND PUBLIC SERVICES

President, Silicon Valley Engineering Council 2002-2003

ASEE (American Society for Engineering Education) Public Policy Committee 2003- Present

State of California Leader for ASEE Engineering Deans Capitol Hill visit 2003, 2004, 2005

Member, NSF Review Panel for Science, Technology, Engineering, and Mathematics (STEM) Education 2004

International Reviewer, National Science and Engineering Research Council of Canada 2004

Member, Advisory Committee for California Summer Mathematics and Science (COSMOS) Education 2004

Member, Advisory Committee for California Mathematics Engineering Science Achievement (MESA) 2004

Member, Advisory Committee for MentorNet 2005

Member, Blue Ribbon Task Force for Nanotechnology, Federal and State of California Initiative, 2005

GRANT SUPPORT (partial since 1993)

2005-2007	Optimization of Self Reverse Biasing Logic for Leakage Reduction	UC, ZTI	\$148,800
1999-2005	Physical CAD	NSF	\$150,000
2002-2005	Low Power Design of Dynamic Circuits	Intel Corp.	\$120,000
2003-2008	Developing Effective Engineering Pathways	NSF	\$2,000,000
2004-2006	Modeling and Simulation of Nanowires	NASA	\$120,000
2001-2003	Optoelectronic Modeling and Simulation	DARPA	\$150,000
2001-2004	Robust and Scalable Low Power High Performance VLSI	SRC	\$360,000
2001-2004	Low Power High Performance Static Dynamic Logic	Intel	\$120,000
1997-2000	Temperature-Dependent VLSI Delay Analysis	Intel	\$120,000
1998-2001	Computer -Aided Design of Reliable Deep Submicron VLSI Circuits	SRC	\$180,000
1998-2001	Low-Power High-Performance Circuits for Sub-1V CMOS	SRC	\$180,000
1998-2000	ESD Protection for BiCMOS RF Circuits	Motorola	\$100,000
1998-2000	Composite CAD for MEMS	DARPA	\$110,000
1998-2000	ESD Protection Circuits	LG Semicon	\$100,000
1999-2000	SD-Induced On-Chip Termination Resistor Variation And Its Impact on I/O Circuit Performance Degradation	SRC	\$ 50,000
1997-1999	I/O Layout Extraction	TI	\$ 80,000
1996-1997	Electrothermal Analysis	Intel	\$ 40,000
1997-1998	MPEG4 VLSI Engine	ETRI	\$100,000
1996-1997	MPEG VLSI	LG	\$100,000
1995-1998	VLSI Research	Hwagoksangsa	\$150,000

1995-1998	VLSI Interconnect Reliability	TI	\$300,000
1994-1995	Modeling and Simulation for VLSI Reliability	SRC	\$ 65,000
1986-1996	Design and Analysis of Optoelectronic System Testbed	NSF ERC	\$1M+
1994-1997	Reliability CAD System	AF Rome Lab	\$180,000
1995-1996	MPEG VLSI	ETRI	\$100,000
1996-1997	Modeling, Simulation and Design Guidelines	SRC	\$ 65,000
1996-1997	Computer Simulation of Optical Interconnects	DARPA	\$ 55,000
1995-1996	Reliability CAD System	AF Rome	\$100,000
1995-1996	Electrothermal Simulation of VLSI	Intel Corp.	\$ 40,000
1995-1996	Electrothermal Stress Tolerant Deep Submicron Low Power Circuits	JSEP	\$ 60,000
1995-1996	Modeling and Simulation for VLSI Reliability	SRC	\$ 65,000
1991-1995	High Level Simulation of VLSI	Samsung Electron Co.	\$400,000
1994-1995	Computer Simulation of Optical Interconnects	ARPA	\$ 65,000
1995-1996	Computer Simulation of Optical Busses	ARPA	\$ 50,000
1995-1996	Design Guidelines for EOS/ESD Reliability	TI	\$ 30,000
1995-1996	Computer Simulation of Optical Busses	ARPA	\$ 65,000
1995-1996	Design Guidelines for EOS/ESD Reliability	TI	\$ 30,000
1994-1995	VLSI Layout Automation	Goldstar Electron Co.	\$ 50,000
1994-1995	Electrothermal Simulation of VLSI	Intel Corp.	\$ 40,000
1994-1995	CAD for Optoelectronics	ETRI	\$100,000
1993-1994	Timing Driven VLSI Layout Automation	Goldstar	\$ 50,000
1994-1995	Design Guidelines for ESD/EOS	TI	\$ 30,000

	Reliability		
1994-1995	ATM Network Research	AT&T	\$ 60,000
1993-1994	Computer Simulation of Optical Busses	ARPA	\$ 65,000
1993-1994	ESD/EOS Reliability Analysis	Intel	\$ 50,000
1993-1994	ESD/EOS Simulation	ESD/EOS Society	\$ 10,000
1993-1994	Design Guidelines for EOS/ESD Reliability	Texas Instruments	\$ 40,000
1993-1994	VLSI Layout Synthesis	Motorola	\$ 45,000
1993-1994	Modeling and Simulation for VLSI Reliability	SRC	\$ 67,000
1993-1994	Computer-Aided Design of High-Performance VLSI Circuits	JSEP	\$ 40,000
1993-1994	VLSI Reliability	AMD	\$ 50,000

PATENTS

1. U.S. Patent 4,396,994, Data shifting and rotating apparatus, August 2, 1983
2. U.S. Patent 5,404,041, Source contact placement for efficient ESD/EOS protection in grounded-substrate MOS ICs, April 4, 1995
3. U.S. Patent 5,450,267, New ESD/EOS protection circuits for integrated circuits fabricated in advanced n-well CMOS processes, September 12, 1995
4. U.S. Patent 5,610,774, Optical communications and interconnection networks having optoelectronic switches and direct optical routers, March 11, 1997
5. U.S. Patent 5,796,638, Methods, apparatus and computer program products for synthesizing integrated circuits with electrostatic discharge capability and correcting ground rules faults therein, August 18, 1998.
6. U.S. Patent, 5,923,656, Scalable broadband input-queued ATM switch including weight driven cell scheduler, July 13, 1999
7. US Patent 6,624,665, CMOS Skewed Static Logic and Method of Synthesis, Sept. 23, 2003
8. US Patent 6,759,873, Reverse Biasing Logic Circuit, July 6, 2004
9. US Patent 6,784,707, Delay Locked Loop Clock Generator, August 31, 2004

10. US Patent 6,784,694, CMOS Sequential Logic Configuration for a Double-Edge Triggered Flip-Flop, August 31, 2004
11. US Patent 6,794,903, CMOS Parallel Dynamic Logic and Speed Enhanced Static Logic, Sept. 21, 2004
12. US Patent 6,900,690, Low Power High Performance Integrated Circuit and Related Methods, May 31, 2005
13. US Patent Approved, Low Power High-Performance Storage Circuitry and Related Methods, Aug. 2002 (UCSC)
14. US Patent Application Filed, Circuit and Method for Event Driven Dynamic Logic, Jan. 2003 (UCSC) (Serial No. 10/325,594)

PUBLICATIONS

Books

1. Y. Leblebici and S. M. Kang, Hot-Carrier Reliability of MOS VLSI Circuits, Kluwer Academic Publishers 1993.
2. S. Sapatnekar and S. M. Kang, Design Automation for Timing-Driven Layout Synthesis, Kluwer Academic Publishers 1993.
3. M. Sriram and S. M. Kang, Physical Design for Multichip Modules, Kluwer Academic Publishers 1994.
4. C. H. Diaz, S. M. Kang and C. Duvvury, Modeling of Electrical Overstress in Integrated Circuits, Kluwer Academic Publishers 1994.
5. S. M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, McGraw-Hill, 1995.(Chinese Translation)
6. J. J. Morikuni and S. M. Kang, Computer-Aided Design of Optoelectronic Integrated Circuits and Systems, Prentice Hall 1996.
7. S. M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, McGraw-Hill, Second Edition, 1998. (Chinese Translation)
8. Y. K. Cheng, C. H. Tsai, C. C. Teng, and S. M. Kang, Electrothermal Analysis of VLSI Systems, Kluwer Academic Publishers, 2000.
9. S. M. Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, McGraw-Hill, Third Edition, 2003 (Chinese Translation)

Books Edited or Co-Edited

Co-Editor, Series in Advances in Design and Analysis of VLSI Systems, Elsevier Science Publishers B. V.
Chapter Editor, Computer-Aided Design and Optimization, The Circuits and Filters Handbook, CRC Press
1995

Chapter Editor, VLSI and ASIC, VLSI Handbook, CRC Press, 1999

Section Editor, The Circuits and Filters Handbook, Section VII, Computer-Aided Design and Optimization,
CRC Press, 2003, pp. 1245-1356

Chapters in Books

1. S. M. Kang and H. Y. Chen, "Circuit Optimization for CMOS VLSI," book chapter, *Advances in Computer-Aided Engineering Design*, JAI Press, Inc., pp. 107-157, 1990.
2. P. Gee, M. Y. Wu, I. N. Hajj, S. M. Kang and W. Shu, "Automatic Circuit Synthesis Using Switching Network Logic and Metal-metal Matrix Layout," JAI Press, Inc., pp. 57-106, 1990.
3. S. M. Kang and M. Sriram, "Binary Techniques for Placement and Routing," book chapter, *Algorithmic Aspects of VLSI Layout*, World Scientific, pp. 25-68, 1994
4. S. M. Kang and A. Dharchoudhury, "Modeling of Circuit Performances," book chapter, pp. 1375-1391, *The Circuits and Filters Handbook*, CRC Press, 1995.
5. C. W. Kim and S. M. Kang, "Low Power Flip-Flop and Clock Network Design Methodologies in High-Performance System-on-Chips (SOCs), Chapter 7, pp. 151-179, *Power Aware Design Methodologies* (M. Pedram, editor), 2002
6. K. W. Kim and S. M. Kang, "Signal Integrity Effects in Custom IC and ASIC Designs," Ramionderpal Singh (editor), IEEE Press, Piscataway, NJ and Wiley-Interscience, New York, NY, 2002

Refereed Journals

1. P. Scott and S. M. Kang, "Stability Properties of a Purkinje Fiber Model," *Computers in Biology and Medicine*, vol. 4, pp. 19-25, June 1974.
2. L. O. Chua and S. M. Kang, "Memristive Devices and Systems," *Proceedings of the IEEE*, Vol. 64, No. 2, pp. 209-223, February 1976.
3. S. M. Kang, "Comments on a Method of Obtaining System Functions Using Δ -M," *Proceedings of the IEEE*, Vol. 65, No. 3, pp. 494, March 1977.
4. L. O. Chua and S. M. Kang, "Sectionwise Piecewise-Linear Functions: Canonical Representation Properties and Applications," *Proceedings of the IEEE (Special Issue on Multidimensional Systems)*, Vol. 65, No. 6, pp. 915-929, June 1977.
5. S. M. Kang and L. O. Chua, "A Global Representation of Multidimensional Piecewise-Linear Functions," *IEEE Transactions on Circuits and Systems*, vol. CAS-25, No. 11, pp. 938-940, November 1978.
6. S. M. Kang, Y. Chen, and T. G. Marshall, Jr., "An Optimal Design of Split-Electrode CCD Transversal Filters," *IEEE Transactions on Circuits and Systems*, Vol. CAS-27, No. 6, pp. 445-451, June 1980.

7. S. M. Kang, "An Optimal Design of Large-Scale Communication Networks," *IEEE Transactions on Circuits and Systems*, pp. 1169-1175, December 1980.
8. S. M. Kang, "A Design of CMOS Polycells for LSI Circuits," *IEEE Transactions on Circuits and Systems*, Vol. CAS-28, No. 8, pp. 838-843, August 1981.
9. S. M. Kang, R. H. Krambeck, H. F. Law, and A. D. Lopez, "Gate Matrix Layout of Random Control Logic in a 32-bit CMOS CPU Chip Adaptable to Evolving Logic Design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. CAD-2, No. 1, pp. 18-29, January 1983.
10. S. M. Kang, "Simulation of Power Dissipation in VLSI Circuits," *IEEE Journal of Solid-State Circuits*, vol. SC-21, no. 5, pp. 889-891, October 1986.
11. S. M. Kang, "Domino CMOS Barrel Switch for 32-Bit VLSI Processors," *IEEE Circuits and Devices*, vol. 3, no. 3, pp. 3-8, May 1987.
12. S. M. Kang, "Physical Design of Microprocessors," *IEEE Design and Test of Computers*, vol. 4, no. 3, pp. 10-11, June 1987.
13. S. M. Kang, "Metal-Metal Matrix- N^3 for High-Speed VLSI Layout," *IEEE Transaction on Computer-Aided Design*, vol. CAD-6, no. 5, pp. 886-891, September 1987.
14. T. K. Yu, S. M. Kang, I. N. Hajj and T. N. Trick, "Statistical Performance Modeling and Parametric Yield Estimation of MOS VLSI," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. CAD-6, no. 6, pp. 1013-1022, November 1987.
15. D. K. Hwang, W. K. Fuchs and S. M. Kang, "An Efficient Approach to Gate Matrix Layout," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. CAD-6, no. 5, pp. 802-809, December 1987.
16. M. E. Mokari-Bolhassan and S. M. Kang, "Analysis and Correction of VLSI Delay Measurement Errors due to Transmission Line Effects," *IEEE Trans. on Circuits and Systems*, vol. CAS-35, no. 1, pp. 19-25, January 1988.
17. W. Shu, M. Y. Wu, and S. M. Kang, "Improved Net Merging Method for Gate Matrix Layout," *IEEE Transactions on Computer-Aided Design*, vol. CAD-7, no. 9, pp. 947-951, September 1988.
18. W. J. Welch, T. K. Yu, S. M. Kang, and J. Sacks, "Computer Experiments for Quality Control by Parameter Design," *Journal of Quality Technology*, vol. 22, no. 1, pp. 15-22, Jan. 1990.
19. S. M. Kang and H. Y. Chen, "A Global Delay Model for Domino CMOS Circuits," *International Journal on Circuit Theory and Applications*, vol. 18, no. 3, pp. 289-306, May 1990.
20. D. S. Gao, A. T. Yang, and S. M. Kang, "Accurate Modeling and Simulation of Interconnection Delays and Crosstalks in High-Speed Integrated Circuits," *IEEE Transaction on Circuit and Systems*, vol. 37, no. 1, pp. 1-9, January 1990.
21. P. Gee, M. Y. Wu, S. M. Kang, and I. N. Hajj, "A Metal-Metal Cell Generator for Multi-Level Metal MOS Technology," *Integration, the VLSI Journal*, vol. 9, no. 1, pp. 25-47, February 1990.
22. D. S. Gao, S. M. Kang, R. P. Bryan, and J. J. Coleman, "Modeling of Quantum Well Laser for Computer-Aided Analysis of Optoelectronic Integrated Circuits," *IEEE Transaction on Quantum Electronics*, vol. 37, no. 7, pp. 1206-1216, July 1990.
23. P. Gee, M. Y. Wu, S. M. Kang, and I. N. Hajj, "Automatic Synthesis of Metal-Metal Matrix Layout," *Int. J. of Comput.-Aided VLSI Des.*, Vol. 2, no. 1, pp. 83-104, 1990.

24. C. H. Diaz, S. M. Kang and Y. Leblebici, "An Accurate Analytical Delay Model for BiCMOS Driver Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 10, no. 5, P. Gee, M. Y. Wu, I. N. Hajj, S. M. Kang and W. Shu, "Automatic Circuit Synthesis Using Switching Network Logic and Metal-metal Matrix Layout," JAI Press, Inc., pp. 57-106, 1990.
25. A. T. Yang, S. M. Kang, and G. C. Yang, "An Integrated System for Device Model Design, Circuit Simulation, and Parameter Extraction," *Advances in Electrical Engineering, Electrosoft Journal*, (ed. P. P. Silvester), pp. 31-43, Computational Mechanics Publications Springer-Verlag, 1990.
26. D. Zhou, F. P. Preparata, and S. M. Kang, "Interconnection Delay in Very High-Speed VLSI," *IEEE Trans. on Circuits and Systems*, vol. 38, no. 7, pp. 779-790, July 1991. (**IEEE Darlington Paper Award**)
27. P. Duchene, M. Declercq, and S. M. Kang, "A Simple CMOS Transition Accelerator Circuit," *Electronics Letters*, pp. 300-301, February 1991.
28. H. Y. Chen and S. M. Kang, "iCOACH: A Circuit Optimization Aid for CMOS High-Performance Circuits," *Integration, the VLSI Journal*, vol. 10, no. 2, pp. 185-212, January 1991.
29. H. Y. Chen and S. M. Kang, "A New Circuit Optimization Technique for High Performance CMOS Circuits," *IEEE Trans. on Computer-Aided Design*, vol. 10, no. 5, pp. 670-677, May 1991.
30. T. K. Yu, S. M. Kang, W. Welch, and J. Sacks, "Parametric Yield Optimization of CMOS Analog Circuits by Quadratic Statistical of Circuit Performance Models," *International Journal of Circuit Theory and Applications*, vol. 19, pp. 579-592, November 1991.
31. G. M. Tharakan and S. M. Kang, "A New Design of a Fast N-Bit Barrel Switch Network," *IEEE Journal of Solid-State Circuits*, Vol. 27, no. 2, pp. 217-221, February 1992.
32. Y. Leblebici and S. M. Kang, "Modeling of nMOS Transistors for Simulation of Hot-Carrier Induced Device and Circuit Degradation," *IEEE Trans. on Computer-Aided Design*, vol. 11, no. 2, pp. 235-246, February 1992.
33. A. Ketterson, M. Tong, J.-W. Seo, K. Nummila, J. Morikuni, K. Y. Cheng, I. Adesida, and S. M. Kang, "A Submicron Pseudomorphic MODFET-based OEIC Receiver," *IEEE Photonics Technology Letters*, vol. 4, no. 1, pp. 73-76, January 1992.
34. A. Ketterson, M. Tong, J. W. Tong, K. Nummila, J. Morikuni, S. M. Kang, and I. Adesida, "A high-performance AlGaAs/InGaAs/GaAs pseudomorphic MODFET-based monolithic optoelectronic receiver," *IEEE Photonics Tech. Lett*, p. 73, 1992.
35. A. Ketterson, M. Tong, J. W. Tong, K. Nummila, K. Y. Cheng, J. Morikuni, S. M. Kang and I. Adesida, "Submicron modulation-doped field-effect-transistor/metal-semiconductor-based optoelectronic integrated circuit receiver fabricated by direct-write electron beam lithography," *J. of Vac. Sci. and Tech. B10*, p. 2936, 1992.
36. J. J. Morikuni, D. S. Gao, and S. M. Kang, "Modeling of Optical Logic Gates for Computer Simulation," *IEE Proceedings-J, Optoelectronics*, vol. 139, no. 2, pp. 105-116, April 1992.
37. Y. H. Shih and S. M. Kang, "Analytic Transient Solution of General MOS Circuit Primitives," *IEEE Transactions on Computer-Aided Design*, vol. 11, no. 6, pp. 719-731, June 1992.
38. C. H. Diaz and S. M. Kang, "New Algorithms for Circuit Simulation of Device Breakdown," *IEEE Trans. on Computer-Aided Design*, vol. 11, no. 11, pp. 1344-1354, Nov. 1992.
39. R. Thaik, N. Lek, and S. M. Kang, "A New Global Router using Zero-One Linear Integer Programming Techniques for Sea-of-Gates and Custom Logic Arrays," *IEEE Transactions on Computer-Aided Design*, vol. 11, no. 12, pp. 1479-1494, Dec. 1992.

40. J. J. Morikuni and S. M. Kang, "An Analysis of Inductive Peaking in Photoreceiver Design," *IEEE Journal of Lightwave Technology*, vol. 10, no. 10, pp. 1426-1437, Oct. 1992.
41. E. C. Chang and S. M. Kang, "Computationally Efficient Simulation of Lossy Transmission Line by Using Numerical Inverse Laplace Transform," *IEEE Trans. on Circuits and Systems*, (Spec. issue on Simulation, Modeling, and Electrical Design of High-Speed and High-Density Interconnects), vol. 39, no. 22, pp. 861-868, November 1992.
42. M. S. Unlu, Y. Leblebici, S. M. Kang, and H. Morkoc, "Transient Simulation of Resonant Cavity Enhanced heterojunction Photodiodes Under Pulse Illumination," *IEEE Photonics Technology Letters*, vol. 4, no. 12, pp. 1366-1369, December 1992.
43. S. G. Bishop, I. Adesida, J. J. Coleman, T. A. DeTemple, M. Feng, K. Hess, N. Holonyak, Jr., S. M. Kang, G. E. Stillman, and J. T. Verdeyen, "The Engineering Research Center for Compound Semiconductor Microelectronics," *Proc. of the IEEE*, vol. 81, no. 1, pp. 132-151, January 1993.
44. Y. Leblebici, W. Sun, and S. M. Kang, "Parametric Macromodeling of Hot-Carrier Induced Dynamic Degradation in MOS VLSI Circuits," *IEEE Transactions on Electron Devices*, vol. , no. 40, no. 3, pp. 673-676, March 1993.
45. Y. Leblebici and S. M. Kang, "Modeling and Simulation of Hot-Carrier Induced Device Degradation in MOS Circuits," *IEEE Journal of Solid-States Circuits*. vol. 28, no. 5, pp. 585-595, May 1993.
46. Y. H. Shih, Y. Leblebici, and S. M. Kang, "ILLIADS: A Fast Timing and Reliability Simulator for Digital MOS Circuits," *IEEE Trans. on Computer-Aided Design*, vol. 12, no. 9, pp. 1387-1402, November 1993.
47. A. A. Ketterson, J. -W. Seo, M. Tong, K. Nummila, J. J. Morikuni, K.-Y. Cheng, S. M. Kang, and I. Adesida, "A MODFET-Based Optoelectronic Integrated Circuit Receiver for Optical Interconnects," *IEEE Trans. on Electron Devices*, vol. 40, no.8, pp. 1406-1446, August 1993.
48. S. Sapatnekar, V. B. Rao, P. M. Vaidya, and S. M. Kang, "An Transistor Sizing Problem for CMOS Circuits Using Convex Optimization," *IEEE Trans. on Computer-Aided Design*, vol. 12, no. 11, pp. 1621-1634, November 1993.
49. C. H. Diaz, C. Duvvury, S. M. Kang, and L. Wagner, "Electrical Overstress Power Profiles: A Guideline to Qualify EOS Hardness of Semiconductor Devices," *Journal of Electrostatics*, vol. 31, pp. 161-176, November 1993.
50. C. H. Diaz, S. M. Kang, and C. Duvvury, "Electrical Overstress Thermal Failure Simulation for Integrated Circuits," *IEEE Transactions on Electron Devices*, vol. 41, no. 3, pp. 359-366, Mar. 1994.
51. C. H. Diaz and S. M. Kang, "Circuit-Level Electro-Thermal Simulation of Electrical Overstress Failures in Advanced MOS I/O Protection Devices," *IEEE Trans. on Computer-Aided Design*, vol. 13, no. 4, pp. 482-493, April 1994.
52. Y. Leblebici and S. M. Kang, "Simulation of Hot Carrier Induced MOS Circuit Degradation for VLSI Reliability Analysis," *IEEE Transactions on Reliability*, vol. 43, no. 2, pp. 197-206, June 1994.
53. J. J. Morikuni, A. Dharchoudhury, Y. Leblebici, and S. M. Kang, "Improvements to the Standard Theory of Photoreceiver Noise," *IEEE J. Of Lightwave Technology*, vol. 12, no. 7, pp. 1174-1184, July 1994.
54. S. S. Sapatnekar, P. M. Vaidya, and S. M. Kang, "Convexity-Based Algorithms for Design Centering," *IEEE Transactions on Computer-Aided Design*, vol. 13, no. 12, pp. 1536-1549, December 1994.

55. C. H. Diaz, C. Duvvury, and S. M. Kang, "Studies of EOS Susceptibility in 0.6 μ m nMOS ESD I/O Protection Structures," *Journal of Electrostatics*, 33 (1994), pp. 273-289.
56. R. M. Lammert, P. V. Mena, D. V. Forbes, M. L. Osowski, S. M. Kang, and J. J. Coleman, "Strained-Layer in GaAs-AlGaAs Lasers with Monolithically Integrated Photodiodes by Selective-Area MOCVD," *IEEE Photonics Tech. Lett.*, Vol. 7, no. 3, pp. 247-250, March 1995.
57. D. H. Cho, S. M. Kang, K.-H. Kim, and S.-H. Lee, "An Accurate Intrinsic Capacitance Modeling for Deep Submicron MOSFETs," *IEEE Trans. on Electron Devices*, Vol. 42, no. 3, pp. 540-548, March 1995.
58. A. Dharchoudhury and S. M. Kang, "Worst-Case Analysis and Optimization of VLSI Circuit Performances," *IEEE Trans. on Comput.-Aided Des.*, Vol. 14, no. 4, pp. 481-492, April 1995.
59. B. K. Whitlock, J. J. Morikuni, E. Conforti, and S. M. Kang, "Simulating Optical Interconnects," *IEEE Circuit and Devices*, Vol. 11, no. 3, pp. 12-18, May 1995.
60. J. Lockwood, H. Duan, J. J. Morikuni, S. M. Kang, S. Akkineni, and R. H. Campbell, "Scalable Optoelectronic ATM Networks: The iPOINT Fully Functional Testbed," *IEEE J. of Lightwave Technol.*, Vol. 13, no. 6, pp. 1093-1103, June 1995.
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199. C. H. Tsai and S. M. Kang, "Fast Temperature Calculation for Transient Electrothermal Simulation by Mixed Frequency/Time Domain Thermal Model Reduction," *ACM/IEEE Design Automation Conf. (DAC)*, Los Angeles, CA, June 5-9, 2000.
200. K. W. Kim, S. O. Jung, U. Narayana, C. L. Liu, and S. M. Kang, "Noise-Aware Power Optimization for On-Chip Interconnect," *International Symp. On Low Power Electronics and Design*, Rappallo, Italy, July 26-27, 2000.
201. J. Chen and S. M. Kang, "Model-Order Reduction of Weakly Nonlinear Systems with Taylor Series Expansion and Arnoldi Approach," *IEEE 43rd Midwest Symp. On Circuits and Systems*, Lansing, MI, Aug. 8-11, 2000.
202. K. H. Baek, K. W. Kim and S. M. Kang, "A Low Energy Encoding Technique for Reduction of Coupling Effects in SoC Interconnects," *IEEE 43rd Midwest Symp. On Circuits and Syst.*, Lansing, MI, Aug. 8-11, 2000.
203. J. Moorman, J. Lockwood and S. M. Kang, "Real-Time Prioritized Call Admission Control in a Base Station Scheduler," *ACM WOWMOM*, Boston, MA, Aug. 2000, pp. 28-37.
204. C. W. Kim, J. S. Lee, K. H. Baek, E. Martina, and S. M. Kang, "High-Performance Low-Power Skewed Static Logic in Very Deep-Submicron (VDSM) Technology," *IEEE Int. Conf. On Comp. Des.*, Austin, TX, Sept. 17-20, 2000, pp. 59-64.
205. C. W. Kim, J. S. Lee, K. H. Baek, and S. M. Kang, "Low-Power Skewed Static Logic with Topology-Dependent Dual V_t ," *13th Annual IEEE Int. ASIC/SOC Conf.*, Washington, DC, Sept. 13-25, 2000, pp. 310-314.
206. S. Joshi, P. Juliano, E. Rosenbaum, G. Kaatz, and S. M. Kang, "ESD Protection for BiCMOS Circuits," *Proc. of IEEE Bipolar/BiCMOS Circuits and Technol. Mtg.*, Minneapolis, MN, Sept. 24-26, 2000, pp. 218-221.
207. J. S. Lee, Y. J. Huh, P. Bendix, and S. M. Kang, "Chip-Level Simulation for CDM Failures in Multi-Power ICs," *EOS/ESD Symp.*, Anaheim, CA, September 26-28, 2000. (**Best Student Paper Award**)
208. K. W. Kim, K. H. Baek, N. Shanbhag, C. L. Liu, and S. M. Kang, "Coupling-Driven Signal Encoding Schemes for Low-Power Interface Design," *IEEE Int. Conf. On Comput.-Aided Design*, San Jose, CA, Nov. 5-9, 2000, pp. 318-321.
209. S. Bucheli, J. R. Moorman, J. W. Lockwood, and S. M. Kang, "Compensation Modeling for QoS Support on a Wireless Network," *Globecom 2000*, San Francisco, CA, Nov. 2000.
210. J. Zhou, C. Liu, J. H. Chen, and S. M. Kang, "Development of a Wide Tuning Range MEMS Tunable Capacitor for Wireless Communication Systems," *IEEE Int. Electron Device Meeting*, 2000.
211. J. H. Chen and S. M. Kang, "Computer-Aided Design of Mixed-Technology VLSI Systems," *IEEE Asia-Pacific Conf. On Circuits and Systems*, Tianjin, China, Dec. 2000.
212. J. H. Chen, J. Zou, S. M. Kang, and C. Liu, "Electro-Mechanical and Microwave S-Parameter Properties Of a Wide-Tuning Range MEMS Tunable Capacitor," *IEEE Conf. On Modeling and Simulation of Microsystems*, Hilton Head Island, SC, Mar. 19-21, 2001.
213. S. O. Jung, K. W. Kim and S. M. Kang, "Transistor Sizing for Reliable Domino Logic Design in Dual Threshold Voltage Technologies," *ACM 11th Great Lakes Symp. On VLSI*, West Lafayette, IN, Mar. 22-23, 2001.

214. S. M. Yoo, S. O. Jung and S. M. Kang, "Two-Level LFSR Scheme with Asynchronous Test Pattern Transfer For Low Cost and High Efficiency Built-In-Self-Test," *ACM 11th Great Lakes Symp. On VLSI*, West Lafayette, IN, Mar. 22-23, 2001.
215. S. O. Jung, K. W. Kim and S. M. Kang, "Noise Constrained Power Optimization for Dual Vt Domino Logic," *IEEE Int. Symp. On Circuits and Systems*, Sydney, Australia, May 6-9, 2001.
216. J. H. Chen and S. M. Kang, "Model-Order Reduction of Nonlinear MEMS Devices Through Arclength-Based Karhunen-Loeve Decomposition," *IEEE Int. Symp. on Circuits and Systems*, Sydney, Australia, May 6-9, 2001.
217. S. M. Yoo, C. W. Kim, S. O. Jung, K. H. Baek, and S. M. Kang, "New Current-Mode Sense Amplifiers for High Density DRAM and PIM Architectures," *IEEE Int. Symp. On Circuits and Systems*, Sydney, Australia, May 6-9, 2001.
218. S. M. Yoo, S. O. Jung and S. M. Kang, "Low Cost and High Efficiency BIST Scheme with 2-Level LFSR and ATPT," *IEEE Int. Symp. On Circuits and Systems*, Sydney, Australia, May 6-9, 2001.
219. K. W. Kim and S. M. Kang, "A Low-Power Reduced Swing Single Clock Flip-Flop," *IEEE Int. Symp. on Circuits and Systems*, Sydney, Australia, May 6-9, 2001.
220. Q. Li, Y. J. Huh, J. W. Chen, P. Bendix, and S. M. Kang, "Full Chip ESD Design Rule Checking," *IEEE Int. Symp. On Circuits and Systems*, Sydney, Australia, May 6-9, 2001.
221. Q. Li, Y. J. Huh, J. W. Chen, P. Bendix, and S. M. Kang, "ESD Design Rule Checker," *IEEE Int. Symp. on Circuits and Systems*, Sydney, Australia, May 6-9, 2001.
222. C. W. Kim, K. W. Kim and S. M. Kang, "Energy Efficient Skewed Static Logic Design with Dual Vt," *IEEE Int. Symp. on Circuits and Systems*, Sydney, Australia, May 6-9, 2001.
223. K. W. Kim, S. O. Jung and S. M. Kang, "Coupling-Aware Minimum Delay Optimization for Domino Logic Circuits," *IEEE Int. Symp. on Circuits and Systems*, Sydney, Australia, May 6-9, 2001.
224. Q. Li and S. M. Kang, "Efficient Algorithms for Polygon to Trapezoid-to- Simple Polygon Decomposition for Resistance Extraction," *IEEE Int. Symp. on Circuits and Systems*, Sydney, Australia, May 6-9, 2001.
225. J. S. Lee, Y. J. Huh, P. Bendix, and S. M. Kang, "Design-for-ESD Reliability in High-Frequency I/O Interfaces in Deep-Submicron CMOS Technology," *IEEE Int. Symp. on Circuits and Systems*, Sydney, Australia, May 6-9, 2001.
226. C. W. Kim and S. M. Kang, "A Low-Swing Clock Double-Edge Triggered Flip-Flop," *IEEE Symp. on Circuits*, June 2001.
227. K. W. Kim, S. O. Jung, P. Saxena, C. L. Liu and S. M. Kang, "Coupling Delay Optimization by Temporal Decorrelation Using Dual Threshold Voltage Technique," *ACM/IEEE Design Automation Conf.*, Las Vegas, NV, June 2001.
228. S. M. Kang and S. M. Yoo, "Circuit Solutions for Overcoming Ultra-Deep Submicron CMOS Leakage Currents, Noises and Power Consumption," *Proc. of Int. Tech. Conf. On Circuits, Systems, Computers and Communications (ITC-CSCC)*, July 10-12, 2001, Tokushima, Japan, pp. 1-4. **(keynote talk)**
229. J. S. Lee, Y. J. Huh, P. Bendix, and S. M. Kang, "Understanding and Addressing the Noise Induced by ESD in Multiple Power Supply Systems," *IEEE Int. Conf. on Computer Design*, Sept. 24-26, 2001, Austin, TX, pp. 406-411.

230. J. S. Lee, Y. J. Huh, P. Bendix, and S. M. Kang, "Noise-Aware Design for ESD Reliability in Mixed-Signal Integrated Circuits," *IEEE Int. ASIC/SOC Conf.*, Arlington, VA, Sept. 2001, pp. 437-441.
231. J. H. Chen and S. M. Kang, "Dynamic Modeling of MEMS Mirror Devices," *IEEE Electron Devices Meeting (IEDM)*, Washington, DC, Dec. 2001, pp. 41.5.1-41.5.4.
232. I. C. Hwang and S. M. Kang, "A Self-Regulating VCO with Supply Sensitivity $<0.15\%$ -delay/ 1% -Supply," *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, Feb. 3-7, 2002, pp. 140-141.
233. C. W. Kim, I. C. Hwang and S. M. Kang, "Low-Power Small-Area $\pm 7.28\text{pS}$ Jitter 1GHz DLL-Based Clock Generator," *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, Feb. 3-7, 2002, pp. 142-143.
234. S. O. Jung, K. W. Kim and S. M. Kang, "Dual Threshold Voltage Domino Logic Synthesis with Noise and Power Constraints," *Design Automation and Test in Europe (DATE)*, Paris France, March 4-7, 2002
235. S. O. Jung and S. M. Kang, "Skew-Tolerant High Performance Domino Logic," *IEEE Int. Symp. on VLSI*, Pittsburgh, PA, April 2002, pp. 41-46.
236. J. H. Chen, Jun Zou, C. Liu, and S. M. Kang, "Development of a MEMS Vertical Planar Coil Inductor," Fifth International Conf. On Modeling and Simulation of Microsystems, April 22-25, 2002, San Juan, Puerto Rico, pp. 344-347.
237. K. H. Baek, Myung-Jun Choe, Celso Souza, and S. M. Kang, "A Low-Power High-Speed BiCMOS Current Switch with Enhanced Spectral Bandwidth," *IEEE Int. Symp. on Circuits and Systems*, Phoenix, AZ, May 26-29, 2002, pp. 53-56.
238. R. K. Grube, Q. Wang, and S. M. Kang, "Design Limitations in Deep Sub- $0.18\mu\text{m}$ CMOS SRAM Circuits for High Performance On-Chip Cache Applications," IEEE Great Lakes Symposium on VLSI, April 18-20, 2002, pp. 94-97.
239. G. Yang, S. O. Jung, S. H. Kim, and S. M. Kang, "A Low-Power 2.1GHz 32-bit Carry Lookahead Adder Using Dual Path All-N-Logic," IEEE Midwest Symposium on Circuits and Systems, August 4-7, 2002, Tulsa, OK.
240. Y. S. Kim, S. H. Kim, K. H. Baek, S. K. Kim, and S. M. Kang, "Multiple Trigonometric Approximation of Sine-Amplitude for High Speed Direct Digital Frequency Synthesizers," VLSI Symposium, Bombay, India, Jan. 2003.
241. S. Wu and S. M. Kang, "Modeling and Time-Domain Simulation of VSEL Using VHDL-AMS," IEEE Southwest Symposium on Mixed-Signal Design, May 2003.
242. Q. Wang and S. M. Kang, "An Optimal Design of Leak-Proof SRAM Cell Using MCDM Method," SPIE International Symposium on Microelectronics for the New Millennium, May 19-21, 2003, Gran Canaria, Spain, vol. 5117, pp. 478-484.
243. K. H. Baek, M.-J. Choi, E. Merlo, and S. M. Kang, "1-GS/s, 12-bit SiGe BiCMOS D/A Converter for High Speed DDFS," International Symp. on Circuits and Systems, May 25-28, 2003, Bangkok, Thailand
244. K. H. Baek, M.-J. Choi, E. Merlo, and S. M. Kang, "Addressing a High Speed D/A Converter Design for Mixed-Mode VLSI Systems," IEEE Southwest Symp. On VLSI, 2003, pp. 21-26
245. K. H. Baek, M.-J. Choi, and S. M. Kang, "An Efficient Calibration Technique for Systematic Current Mismatch of D/A Converters," International Symp. On VLSI, 2003, pp. 80-84.
246. S. M. Kang (Invited Keynote Address paper), "Elements of Low Power Design for Integrated Systems," IEEE International Symp. On Power Electronics and Design (ISPLED), Aug. 25-27, 2003, Seoul, Korea.

247. S. M. Kang, G. Yang, Q. Wang, and Z. Wang (Invited paper), "Gate Leakage Tolerant Circuits in Deep Sub-100nm CMOS Technologies," SPIE Conf. on Microelectronics, MEMS, and Nanotechnology, Dec. 10-12, 2003, Perth, Australia
248. G. Yang, S. O. Jung, K. H. Baek, S. H. Kim, and S. M. Kang, "1.85 GHz 32-bit Carry Lookahead Adder Using Dual Path All-N-Logic, IEEE International Symposium on Circuits and Systems, May 23, 2004, Van Couver, Canada
249. G. Yang, Z. Wang, and S. M. Kang, "Low Power High Performance Techniques for High Fan-In Dynamic Gates," 5th International Symposium on Quality Electronic Design, pp. 421-424, March 2004, Santa Clara, CA
250. G. Yang, Z. Wang, and S. M. Kang, "Leakage-Proof Domino Circuit for Deep Sub-100nm Technologies," pp. 222-227, Jan. 2004, Mumbai, India
251. S. Wu and S. M. Kang, "Modeling of Metal Semiconductor Metal Photodetector Using VHDL-AMS," IEEE Behavioral Modeling and Simulation Conf. San Jose, Oct. 21-22, 2004
252. G. Yang, Y. S. Kim, and S. M. Kang, "Current Mode Multi-Level Simultaneous Bidirectional I/O Scheme for Chip-to-Chip Communications," IEEE International Symposium on Circuits and Systems, Kobe, Japan, May 23-26, 2005
253. S. H. Shin, K. R. Lee, and S. M. Kang, "Multi- GHz Range Divide-by-2 Circuit Using Modified-TSPC Topology," submitted to IEE Electronics Letters
254. S. H. Shin, K. R. Lee, and S. M. Kang, "3.48mW 2.4GHz Range Frequency Synthesizer Architecture with Two-Point Channel Control for Fast Settling Performance," IEEE System-on-Chip Conference, September, 2005, Santa Clara, CA
255. S. Kim and S. M. Kang, "A Fast Algorithm for Leakage Current Estimation," submitted to IEEE International Conference Computer-Aided Design, 2005
256. P. Holm, J. H. Park, and S. M. Kang, "Leakage Reduction in CMOS VLSI Logic by Self Reverse Biasing Method," submitted to International Conference on Computer Design, October 2005

Bulletins

1. A. T. Yang and S. M. Kang, "iSMILE User's Manual," CCSM Report No. 88-62, UILU-ENG-88-0406.
2. J. J. Morikuni and S. M. Kang, "Computer Simulation of Optical Logic Gates," Report to McDonnell-Douglas 1990
3. S. M. Kang and I. N. Hajj, "VLSI Design for Reliability-Hot Electron," Final Project Report to Rome Laboratory, March 1991.
4. C. Diaz and S. M. Kang, "Modeling and Simulation of EOS Failures in IC and Development of Design Guidelines," 4Q91, 1Q92, 2Q92, 3Q92, 4Q92, Report to Texas Instruments, January 1992- December 1992.
5. S. M. Kang, "Computer-Aided Design of Optoelectronic Subsystem," IEEE Report on Packaging, Interconnects, Optoelectronics for the Design of Parallel Computers Workshop, pp. 19-29, Schaumburg, IL, Mar. 1992.

6. M. Sriram and S. M. Kang, "A New Layer Assignment Approach for MCMs," Technical Report UIUC-BI-VLSI-92-01
7. J. J. Morikuni and S. M. Kang, "An Analysis of Inductive Peaking in Photoreceiver Designs," Technical Report UIUC-BI-VLSI-92-02.
8. M. Sriram and S. M. Kang, "Efficient Approximation of Time Domain Response of Lossy Coupled Transmission Line Trees," Technical Report UIUC-BI-VLSI-91-03.
9. Izzet Cem Goknar, Haydar Kutuk, and Sung-Mo (Steve) Kang, "Moment Components: A New Tool for Obtaining Passive Reduced Order Models," CSL Technical Report, # UILU-ENG-98-2224 (DAC-68), October 1998.
10. Ki-Wook Kim, C. L. Liu, and Sung-Mo Kang, "Implication Graph Based Domino Logic Synthesis," CSL Technical Report, UILU-ENG-99-2206 (DAC-72), April 1999.

Magazine Articles and Licenses

1. Engineers Week Message by Silicon Valley Engineering Council President," San Jose Business Journal, Feb. 2003.
2. Engineering a Dream," Santa Cruz Sentinel Newspaper, July 21, 2002
3. 'Foundation for Greatness: Head of UCSC's Engineering School Aims to Build a Top-Rated Program," Santa Cruz Sentinel Newspaper, July 22, 2002
4. "Designing Hot-Carrier Resistant VLSI Circuits," Semiconductor International, Sept. 1991,
5. "The ILLIADS' ODYSSEY," Illinois Quarterly, Jan/Feb. 1991.
6. iSMILE Program, Licensed to University of Illinois
7. ILLIADS Program, Highlighted in Illinois Quarterly, Semiconductor International
8. iEDISON 3.0 Program, Licensed to University of Illinois
9. iETSIM Program, Licensed to University of Illinois and Semiconductor Research Corp.
10. ILLIADS Program, Licensed to University of Illinois and then to Deutsch Research Incorp.
11. iFROST Program, Licensed to University of Illinois and then to RSoft Inc.

UNIVERSITY SERVICE

Circuits and Signal Processing Committee University of Illinois, 1985-1995 (Chair 1991)

University Senate, University of Illinois, 1986-87, 1992-1994

Graduate Committee, Dept. of ECE, University of Illinois, 1986-1989

Graduate Seminar Committee, Dept. of ECE, University of Illinois, 1986-1990, 1992-1994

Research Thrust Leader, NSF Engineering Research Center, University of Illinois, 1987-1996

Associate Director, NSF Engineering Research Center, University of Illinois, 1987-1995

Chairman, Ph.D. Qualifying Examination Committee, University of Illinois, 1988

Department Advisory Committee, University of Illinois, 1988-1989

CSL (Coordinated Science Laboratory) Policy and Planning Committee, University of Illinois, 1989-1990

ICAP (Illinois Computer Affiliates Program) Co-Chairman, University of Illinois, 1990

Chair, Circuits and Signal Processing Area, University of Illinois, 1991-1995

ICAP, Chairman, University of Illinois, 1991

Thrust Leader, Center for Optoelectronics Science and Technology (COST), 1993-1996

Department Head of Electrical and Computer Engineering, University of Illinois, 1995- 2000

Campus Critical Research Initiative Proposal Review Board, University of Illinois, 1995

College Promotion and Tenure Committee, University of Illinois, 1995

Course Director of ECE 382 (Large-Scale Integrated Circuits), University of Illinois, 1985-2000

Course Director of ECE 482 (Physical VLSI Design), University of Illinois, 1986-2000

Chair, Faculty Search Committee, University of Illinois, 1995-2000

Member, Beckman Institute Steering Committee, University of Illinois, 1995-2000

Chair, Tykociner Lecture Committee, University of Illinois, 1996-2000

UC Santa Cruz Dean, Baskin School of Engineering, 2001- present

UC Santa Cruz Board of Trustees (honorary member), 2001- present

UC Santa Cruz Provost Advisory Council, 2001- 2004

UC Santa Cruz Executive Advisory Committee, 2005-present

UC Santa Cruz Advisory Committee for Facilities, 2001-present

UC Santa Cruz MBEST Oversight Committee, 2001-present

UC Santa Cruz Academic Planning Council, 2001- present

UC Santa Cruz Academic Instruction and Research Steering Committee, 2003- present

UC Santa Cruz Communications Advisory Committee, 2002- present

California Institute for Science and Innovation CITRIS Executive Committee, 2001- present

California Institute for Science and Innovation QB3 Executive Committee, 2001- 2003

UC Santa Cruz, Chancellor's Advisory Committee on Educational Partnership Program Chair, 2003- present

UC Santa Cruz Strategic Futures Committee for 2020, 2003-present

UC Santa Cruz Long Range Development Planning Committee, 2003-present

OUTSIDE PROFESSIONAL ACTIVITIES

IEEE Standards Board Liaison Representative - 1977 to 1980

Editorial Board Member, International Journal of Circuit Theory and Applications-1984 to Present

Editor of Physical Design, IEEE Design and Test of Computers - May 1984 to July 1988

ADCOM Member, IEEE Circuits and Systems Society - January 1985 to December 1987

Associate Editor, IEEE Circuits and Devices Magazine - March 1987 to December 1989

Founding Chairman, Technical Comm. on VLSI Systems and Applications, IEEE Circuits and Systems Society - July 1987 to May 1989, May 1993 to December 1994

Secretary and Treasurer, IEEE Circuits and Systems Society - January 1988 to December 1988

Associate Editor, Circuits, Systems and Signal Processing Journal - January 1989-1992

Associate Editor, IEEE Transactions on Circuits and Systems - June 1989 to May 1991

Administrative Vice President, IEEE Circuits and Systems Society, 1989

President-Elect, IEEE Circuits and Systems Society, 1990

President, IEEE Circuits and Systems Society, 1991

IEEE Circuits and Systems Society Fellow Committee, 1991-2002

Member, Steering Committee, IEEE Multichip Module Conference, 1991-1995

NSF Review Panel, 1992 – 1995

Member, IEEE Technical Activities Board Administration Council, 1992

Chair, System Implementation Subcommittee, IEEE Multichip Module Conference, 1992 – 1994

Past President, IEEE Circuits and Systems Society, 1992

Member, IEEE TAB Administration Council, 1992

IEEE Circuits and Systems Society Nominations Committee Chair, 1993

IEEE Computer Society Fellow Committee, 1994

Chair, IEEE Transactions VLSI Systems Best Paper Award Technical Program Committee 1994-1997

Technical Program Chair, IEEE Asia Pacific Conference on Circuits and Systems 1994-1996

Technical Program Chair, IEEE International Symposium on Circuits and Systems 1994-1997

Member, IEEE LEOS Society Engineering Achievement Award Committee 1996

Program Co-Chair, IEEE Great Lakes VLSI Symposium Urbana, IL, 1997

Member Editorial Board, Proc. of the IEEE, 1996-Present

Member, Steering Committee, International Symposium on Physical Design, 1996

Member, Technical Program Committee International Symposium on Physical Design, 1997

Secretary (President Elect), National EE Department Heads Assoc. (NEEDHA), 2000

ASEE Engineering Deans Council, 2001- present

AAAS, 1996- present

Member, ASEE Policy Committee, 2003- present

Chair, IEEE Transactions on VLSI Systems Best Paper Award Committee, 1994-1997

Member, IEEE CAS Meritorious Service Awards Committee 1994-1996

Member, IEEE CAS Education Award Committee 1994-1996

Member Steering Committee, IEEE Multichip Module Conference, 1991-1995

Member, International Steering Committee, IEEE Asia-Pacific Conference on Circuits & Systems, 1991-96

Editorial Board Member, Circuits Systems and Signal Processing, Birkhauser.

Program Committee, Southwest Symp. on Mixed-Signal Des., 1999

Chair, IEEE Circuits and Systems Society Technical Achievement Committee, 1999

Member, Technical Program Committee, IEEE International Symposium on Physical Design, 2002-2003

Member, Technical Program Committee, IEEE International Conf. On Microelectronic Systems Education, 2003

Member, Program Committee, SPIE Conf. on Microelectronics, MEMS, and Nanotechnology, 2003

Founding Member, IEEE-CAS Technical Committee on Nanoelectronics and Giga-Scale Systems, 2003

Member, International advisory committee for SOC Design Conference (SDC), 2003

General Chair, IEEE International Conference on System-On-a-Chip Conference (SOCC), September 2004

Chair, IEEE Circuits and Systems Society Technical Achievements Award Committee, 2004

External Advisory Board Member, Northwestern University, 1997-2000

External Advisory Board Member, Hong Kong University of Science and Technology, 1997-Present

External Review Board Member, Hong Kong Research Grants Council, present

External Review Board, Member, University of Alberta, Canada, 1999

Board Member, NEEDHA (National EE Heads Association) 1999-2000

Member, NSF Board of Visitors, 2000

Member, NSF Career Award Panel, 2002

President, Silicon Valley Engineering Council 2002-2003

State of California Leader for ASEE Engineering Deans Capitol Hill visit 2003, 2004

Member, NSF Review Panel for Science, Technology, Engineering, and Mathematics (STEM) Education, 2004

International Reviewer, National Science and Engineering Research Council of Canada, 2004

Member, Executive Committee, NSF Engineering Research Center for Biomimetic Microelectronic Systems, 2003-

Member, International Advisory Committee, BK21 Program, Republic of Korea, 1998, 2005

Member, Blue Ribbon Task Force for Nanotechnology, Federal and State of California Initiative, 2005

EDITORSHIP OF JOURNALS

Special Guest Editor, Proc. Of the IEEE, On-Chip Thermal Engineering, scheduled for Oct. 2005

Special Guest Editor, Proc. of the IEEE, Interconnections-Addressing the Next Challenge of IC Technology, Part 1, April 2001

Special Guest Editor, Proc. of the IEEE, Interconnections-Addressing the Next Challenge of IC Technology, Part 2, May 2001

Founding Editor-in-Chief, IEEE Trans. on VLSI Systems, 1992-1994

Special Guest Editor, International Journal on Circuit Theory and Applications,
Nov. 1991 Issue

Special Guest Editor, International Journal on Circuit Theory and Applications,
jointly with Professor P. DeWilde in The Netherlands, on Fundamental Methods
for Computer-Aided Design for the October 1988 issue.

Special Guest Editor, IEEE Design and Test of Computers, June 1987 issue on
Physical Design of 32-bit Microprocessors.

Editorial Board Member, International Journal of Circuit Theory and Applications, June 1984-Present

Editor, Physical Design, IEEE Design and Test of Computers, 1984-88

Editorial Board Member, Circuits, Systems and Signal Processing, 1986-Present

Editor of Digital Electronics, IEEE Circuits and Devices Magazine, 1987-1989

Associate Editor, IEEE Transactions on Circuits and Systems, June 1989-May 1991

Associate Editor, Circuits, Systems, and Signal Processing Journal, Jan.
1989-Dec. 1990

Editorial Board Member, Proc. of the IEEE, 1996-Present

International Advisory Board Member, IEICE Trans. On Fundamentals of Electronics, Communications and Computer Sciences, Engineering Sciences Society of Japan, 2000-present

Co-Series Editor, Advances in CAD for VLSI Book Series, Elsevier Science

Reviewer, *IEEE Transactions on Computer-Aided Design of Integrated Circuits*, *IEEE Trans. on Electron Devices*, *IEEE Transactions on Circuits and Systems*, *IEEE Journal of Solid-State Circuits*, *International Journal of Circuit Theory and Applications*, Addison-Wesley Publishing Company, Prentice-Hall, Inc., McGraw-Hill, Springer-Verlag, Princeton Press, NSF

CONSULTING ACTIVITIES

ZMOS Technology Inc., Co-Founder and Chairman, 2002- present

Cadence/Celestry, Chairman, Technical Advisory Board, 2000- present

BTA Technology Inc., Board of Directors, 2000

Rockwell Science Center, Technical Consultant, 2001- 2002

Apache Design Automation, Technical Advisory Board, 2001- present

Avanti Corp. July 1996-1999

Texas Instruments, 1998-1999

Samsung Electron Co., Dec. 1995-May 1996

Anagram Inc. Aug. 1993-July 1996 (Board of Directors)

Teltech, Inc., Aug. 1989-2000

Motorola, Inc. August 1990

MCC, Austin, TX, November 1988

AT&T Bell Laboratories, Allentown, PA, Murray Hill, Holmdel, NJ, Dec. 1988-1990

RESEARCH AREAS

Low Power Digital Integrated Circuits

Application Specific Integrated Circuits (ASICs)

Wafer-level VLSI Reliability

Computer-Aided Design of VLSI Circuits and Systems

Computer-Aided Design of OEICs

OEIC Systems and Optical Interconnects

Fully Optical Networks

Nanoelectronics

GRADUATE THESES COMPLETED (Since 1998):**(a) M.S. Degrees Granted: 41 (partial list)**

J. Moorman	1998
M. Bossardt	1998 Swiss Federal Institute of Technology at Lausanne (Best Thesis Award)
S. Dixon	1998
D. Chen	1999
V. Nishar	1999
J. Katzenstein	2000
G. Yang	2003 UCSC
Q. Wang	2003 UCSC
A. Barangan	2003 UCSC
Z. Wang	2004 UCSC
P. Holm	2005 UCSC

(b) M.S. Thesis Students Supervised at Present: 1

T. Onishi (UCSC)

(c) Ph.D. Degrees Granted (list of last 5 years) 51

K. W. Kim	2000
S. Ho	2000
S. Y. Park	2000
W. C. Choi	2000
C. H. Tsai	2000
J. Moorman	2000
J. H. Chen	2000
J. S. Lee	2001
C. W. Kim	2001
S. M. Yoo	2001
K. H. Baek	2002
S. O. Jung	2002
G. Yang	2004 UCSC
S. Wu	2005 UCSC

(d) Ph.D. Thesis Students Supervised at UCSC: 5

S. Kim
 J. H. Park
 Wei Li
 Jun Hu
 Q. Wang

POST DOCTORAL RESEARCHERS AND VISITORS HOSTED

J. M. Lee, 1991-1992, Korea, Kwandong University

D. Y. Han, 1992-1993, Korea, Kunkook University
Y. Leblebici, 1990-1993, Turkey, Technical University of Istanbul
E. Conforti, 1992-1994, Brazil, University of San Paolo
Y. Leblebici, 1994, 1997, Turkey, Technical University of Istanbul
C. Goknar, 1995-1998, Turkey, Technical University of Istanbul
M. K. Lee, 1996-1997, Yonsei University, Korea
Y. J. Huh, 1997-1998 LG Semicon, Korea
J. Lockwood, 1993-1999, UIUC
I. C. Hwang, 2000-2001, Korea University
H. B. Kim, 2000, Samsung Electron Company
S. W. Kim, 2001-2002, Korea University
S. Kim, 2001-2002, Korea University
J. H. Choi, 2001, Samsung Electron Company
D. Axelrad 2002, University of Grenoble, France
I. Shim, 2002, Korea University
Georg Kriebel, 2002-2003, Swiss Federal Institute of Technology at Lausanne
S. H. Shin, 2004- 2005, Korea Advanced Institute of Science and Technology
S. I. Chae, 2005- present, Seoul National University

OTHER SCHOLARLY ACTIVITIES

Distinguished Lecturer, University of Notre Dame, 1992
Distinguished Lecturer, University of Washington, 1991
Associate in The Center for Advanced Study, UIUC, 1991-1992
NSF Review Panel, Washington, DC, 1992
Distinguished Lecturer, Iowa State University, 1992
Invited Speaker, National Science Foundation Workshop, 1993
Invited Speaker, University of Washington, 1993
Distinguished Lecturer; National Research Council, Republic of China, 1993
Distinguished Lecturer, International Conference on VLSI and CAD, Korea 1993

Plenary Speaker, 1992 EOS/ESD Symposium, Dallas, TX

Invited Speaker, High Speed Interconnects Workshop, Santa Fe, NM, 1993

Invited Speaker, OSA Symposium, Toronto, Canada, 1993

Plenary Speaker, 1995 IEEE International Symposium on Circuits and Systems

Distinguished Lecturer, Asia-Pacific Conference on Circuits and Systems 1994

Distinguished Lecturer, IEEE Circuits and Systems Society 1994-1996

Invited Speaker, SPIE Photonics/East 1994

Technical Program Chair, 1996 IEEE Asia-Pacific Conference on Circuits and Systems, Seoul, Korea

Technical Program Chair, 1997 IEEE International Symposium on Circuits and Systems, Hong Kong

Lecturer, Low Power Memory Design, Monterey, CA, April 1997

Lecturer, Low Power Memory Design, Lausanne, Switzerland, July 1997

Invited Talk, University of Karlsruhe, Germany, July 1997

Invited Talk, National University of Singapore, January 1998

Invited Talk, Korean Advanced Institute of Science and Technology, January 1998

Invited Talk, Technical University of Munich, Germany, July 1998

Invited Talk, Motorola Corp. Munich, Germany, Aug. 1998

Invited Talk, Tsinghua University, China, Dec. 2000

Invited Talk, Tokushima University, Japan, July 2001

Invited Talk, New York Chapter of KSEA, November 2001

Invited Talk, Plenary, "On-chip Thermal Engineering," Int. Symp. on Physical Design, San Diego, CA, Apr. 2001.

Invited Talk, "UCSC School of Engineering," UC Board of Regents, Feb. 2002

Invited Talk, "Three Tenors of Technology for the 21st Century," Korean-American Chamber of Commerce of Silicon Valley, March 28, 2002

Invited Talk, "UCSC Engineering Programs," Cabrillo Kiwanis Club, Aptos, Oct. 2002

Invited Talk, UK House of Lords Science and Technology Committee, "Innovations in Microprocessors," June 10, 2002, Stanford University

Invited Talk, Santa Cruz Technology Symposium Keynote Address, February 23, 2002

Invited Talk, Korean Advanced Institute of Science and Technology (KAIST), June 2002

Invited Talk, "A Brief Highlight of Korean-American Engineers," at Centennial Celebration of Korean Immigration To United States Symposium, August 17, 2002, Falls Church, VA.

Invited Talk, "UCSC Engineering Programs," Cabrillo College, Oct. 23, 2002.

Invited Talk, “Industry-University Collaboration for Curriculum Development,” Stanford University-KAIST Technology Forum, Stanford University, June 17, 2003

Invited Talk, “Building Engineering Programs for the 21st Century,” IEEE Circuits and Systems Chapter Inauguration Meeting, San Jose, CA, June 16, 2003

Invited Talk, C. M. Lee Scholarship Award Ceremony, San Jose, CA, June 28, 2003

Invited Lectures, “Design for Manufacturability,” KAIST, Taejon, Korea, Aug.12, 2003

Invited Talk, Santa Cruz Rotary Club, “Engineering for the 21st Century,” June 3, 2004

Invited Talk, “Micro/Nanoelectronics for Life Systems,” 2004 European Workshop for Microelectronics Education, Swiss Federal Institute of Technology, Lausanne, Switzerland, Apr.14-15, 2004

Invited Lecture, “Elements of Low Power Design,” IEEE Circuits and Systems Society Distinguished Lecturer’s Tour Lecture, Universidad Nacional del Sur, Bahia Blanca, Argentina, Nov. 19, 2004

Invited Talk, “Engineering Education for the 21st Century,” IEEE Education Society-Silicon Valley Chapter, December 1, 2004

Invited Lecture, “Design of Deep Submicron CMOS Circuits for Manufacturability,” European Conference on Circuit Theory and Design, Cork, Ireland, September 2005

PROFESSIONAL IMPROVEMENT

Quality Control Workshop, 1990

University of Illinois Dean’s Undergraduate Advising Workshop, 1993

National Institute of Teaching Effectiveness, June 1993

Dean’s Workshop on Teaching: Tradition vs. Innovation, Oct. 1993

Provost’s New Administrators Orientation Workshop, Sept. 1995

Provost’s Pew Table Workshop, October 1995

Dean’s Workshop on Partnership for Illinois, Nov. 1995

NTU/Undergraduate Teaching Improvement, Jan. 1996

Workshop on Investigation Techniques, Preparation of Findings and Mediation, January 1996

Sexual Harassment Workshop, University of Illinois, 1997

Budget Reform Workshop, University of Illinois, 1997

Presidential Retreat, University of Illinois, 1999

Chancellor’s Retreat, University of California Santa Cruz, 2001, 2002, 2003, 2004

UC Management Institute, 2002